Philippe LOPEZ
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34 years old, single

Electronic Engineer

10 years of experience

Professional Experience

Since 04/2002 — **Development Engineer - Texas Instruments France (Villeneuve-Loubet)**

Team Leader of the Front-End Integration (5 persons):

- Evaluation device and power system definition with the customer.
- Define integration work split, common methodology with the customer (flow and tools).
- Define FE quality requirement on each subsys/top netlists deliveries at each step of the integration phase to fulfill all activities requirements (Verification, DFT & Back-end) during the overall project design cycle.
- Put in place static verification tool such as Spyglass and SOC Connectivity as Spider, Spinner and Naxos. Responsible of all the Front-End Subchip/Top Levels RTL/netlist deliveries to the customer.
- Responsible for all the functional ECOs implementation.

Team Leader of the Validation (5 persons):

- Responsible for the TI Peripherals design, validation and support to the customer. Put in place validation automatic flow.
- Secure verification and STA results correlation. Support timing closure activity and NFECOs solutions.

STA Leader:

- Coordinate the STA results within TI Team. Responsible for all STA constrains updates in TI blocks and communication with the customer.
- Support timing closure activity with the back-end team for delivering fast NFECO.

Responsible on RTL modifications, synthesis, floorplanning, verifications RTL and Gate, STA, X-Talk. MGS3 (TI DSP Core) Testcases in assembler, RTL generation of BIST and Efuse.

08/2000 – 04/2002 — **Development Engineer - ARM France (Sophia Antipolis)**
Responsible of the validation of the CPU ARM720TD (8ko $, MMU, CP, CPU ARM7TDMI) and generation of the ATPG vectors and specific test vectors in the non-scannable area of the device.

11/1999 – 08/2000 — **Development Engineer - EuroMIPS Systems (Sophia Antipolis)**
Subcontractor at TI: Synthesis of blocks, floorplanning, IR Drop study, and flow development for vectors generation.

02/1999 – 07/1999 — **Development Engineer - Thales Computer (Toulon)**
Bridge CPU Power PC validation: PCI 32bits-33MHz, PCI 64bits-66MHz and SDRAM 100-133MHZ or EDO-DRAM 66MHz.

Education

1998 — **Diploma of E.N.S.E.I.R.B.**, Micro-electronic Option. (Bordeaux's National Graduate School of Electronic Engineering) part of the French "Grandes Ecoles". Equivalent MSEE.

1994 — **D.U.T. Génie Electrique et Informatique Industrielle**: 2-year degree in Electrical and Industrial Eng

1992 — **Baccalauréat D.**, French secondary school diploma (Physics, Mathematics and Biology).

Technical skills

Languages	⇨ English: Fluent
Software	⇨ Perl, C; Assembler ARM Architecture v4; VHDL, Verilog
OS	⇨ UNIX, Linux, Windows XP
Connectivity	⇨ Magillem Naxos, Duolog Spider & Spinner
Verification	⇨ Atrenta Spyglass, Cadence LEC; Mentor Modelsim, Cadence NC-Verilog, Synopsys VCS
Synthesis / STA	⇨ Synopsys Design Compiler, Magma BlastRTL; Synopsys PrimeTime & PrimeTime-SI
SCM / DRM	⇨ Atria Rational Clearcase / MatrixOne Synchronicity DesignSync
ATPG	⇨ TetraMAX & Flextest

Personal skills

Sports	**:** Bike, swimming, running, ski, table tennis.
Leisure	**:** Astronomy, photography, travel, hiking.